CLAIMS:

1. A voltage supply structure for an integrated circuit, the integrated circuit comprising one or more logic trees having a plurality of logic paths, each logic path having an associated delay at a particular voltage level, characterized in that the voltage supply structure is partitioned such that the voltage level supplied to a particular logic path is predetermined according to the delay of that logic path.

2. A voltage supply structure as claimed in claim 1, wherein the voltage level for each logic path is selected such that each logic path in the logic tree has substantially the same worst-case delay.

3. A voltage supply structure as claimed in claim 1 or 2, wherein the voltage level supplied to a particular logic path is predetermined such that the worst-case delay at the supplied voltage level matches a clock cycle time of the integrated circuit.

4. A voltage supply structure as claimed in any one of the preceding claims, wherein the voltage level supplied to a particular logic path is lowered compared to a nominal voltage level in the integrated circuit, in proportion to the delay of the logic path at the nominal voltage level.

5. A voltage supply structure as claimed in any one of the preceding claims, wherein the voltage level is lowered in non-critical logic paths.

6. A voltage supply structure as claimed in any one of the preceding claims, wherein a logic tree comprises first and second logic paths, the first and second logic paths sharing an overlapping portion, whereby the overlapping portion of the logic path is duplicated, and wherein the voltage supply structure is partitioned such that the non-overlapping portion of the first logic path and corresponding duplicated portion is supplied a first voltage level, and wherein the non-overlapping portion of the second logic path and corresponding duplicated portion are supplied a second voltage level.

7. A voltage supply structure as claimed in claim 6, whereby an input register to the overlapping portion of the logic path is duplicated, such that the duplicated logic path receives data from the duplicated input register.

8. A voltage supply structure as claimed in claim 7, wherein the input register and duplicate input register are clocked conditionally, such that the input register for a particular path is only clocked at events after which the corresponding path is going to be selected.

9. A voltage supply structure as claimed in any one of claims 6 to 8, wherein the plurality of logic paths are connected at a root of a logic tree.

10. A voltage supply structure as claimed in claim 9, wherein the plurality of logic paths are connected at the root using a multiplexer.

11. A voltage supply structure as claimed in claim 10, wherein the multiplexer is supplied with a voltage level corresponding to the voltage level supplied to the logic path having the worst-case delay.

12. A voltage supply structure as claimed in any one of claims 1 to 5, wherein a logic tree comprises first and second logic paths, the first and second logic paths sharing an overlapping portion, whereby the voltage supply structure is partitioned such that the non-overlapping portion of the first logic path is supplied a first voltage level and the non-overlapping portion of the second logic path is supplied a second voltage level, and wherein the overlapping portion is supplied a voltage level corresponding to the higher of the first and second voltage levels.

13. A voltage supply structure as claimed in claim 12, wherein the first and second logic paths are connected using a level converter at the location where the overlapping portion commences.

14. A voltage supply structure as claimed in any one of the preceding claims, further comprising level converters for interfacing between logic paths having different voltage levels.

15. A method of designing a voltage supply structure for an integrated circuit comprising one or more logic trees having a plurality of logic paths, each logic path having an associated delay at a particular voltage level, the method comprising the steps of:

selecting a logic tree having two or more logic paths with unequal delays;

determining the delay of each logic path in the selected logic tree at a particular voltage level;

partitioning the voltage supply such that the voltage level supplied to each logic path in the logic tree is based on the delay of the logic path.

16. A method as claimed in claim 15, wherein the voltage level for each logic path is selected such that each logic path in the logic tree has substantially the same worst-case delay.

17. A method as claimed in claim 15 or 16, wherein the voltage level supplied to a particular logic path is predetermined such that the worst-case delay at the supplied voltage level matches a clock cycle time of the integrated circuit.

18. A method as claimed in any one of claims 15 to 17, wherein the voltage level supplied to a particular logic path is lowered compared to a nominal voltage level on the integrated circuit, in proportion to the delay of the logic path at the nominal voltage level.

19. A method as claimed in any one of claims 15 to 18, wherein the voltage level is lowered in non-critical logic paths.

20. A method as claimed in any one of claims 15 to 19, whereby a logic tree comprises first and second logic paths, the first and second logic paths sharing an overlapping portion, and further comprising the step of duplicating the overlapping portion of the logic path, and partitioning the voltage supply structure such that the non-overlapping portion of the first logic path and the corresponding duplicated portion is supplied a first

voltage level, and wherein the non-overlapping portion of the second logic path and corresponding duplicated portion are supplied a second voltage level.

21. A method as claimed in claim 20, further comprising the step of duplicating an input register to the overlapping portion of the logic path, such that the duplicated logic path receives data from the duplicated input register.

22. A method as claimed in claim 21, wherein the input register and duplicate input register are clocked conditionally, such that the input register for a particular path is only clocked at events after which the corresponding path is going to be selected.

23. A method as claimed in any one of claims 20 to 22, wherein the plurality of logic paths are connected at a root of a logic tree.

24. A method as claimed in claim 23, wherein the plurality of logic paths are connected at the root using a multiplexer.

25. A method as claimed in claim 24, wherein the multiplexer is supplied with a voltage level corresponding to the voltage level supplied to the logic path having the worst-case delay.

26. A method as claimed in any one of claims 15 to 25, wherein a logic tree comprises first and second logic paths, the first and second logic paths sharing an overlapping portion, further comprising the step of partitioning the voltage supply structure such that the non-overlapping portion of the first logic path is supplied a first voltage level and the non-overlapping portion of the second logic path is supplied a second voltage level, and wherein the overlapping portion is supplied a voltage level corresponding to the higher of the first and second voltage levels.

27. A method as claimed in claim 26, further comprising the step of providing a level converter for connecting the first and second logic paths at the location where the overlapping portion commences.

28. A method as claimed in any one of claims 15 to 27, further comprising the step of providing level converters at interfaces between logic paths having different voltage levels.